Design and optimization of thermo-mechanical reliability in wafer level packaging

X.J. Fan, B. Varia, Q. Han

Abstract

In this paper, a variety of wafer level packaging (WLP) structures, including both fan-in and fan-out WLPs, are investigated for solder joint thermo-mechanical reliability performance, from a structural design point of view. The effects of redistribution layer (RDL), bump structural design/material selection, polymer-cored ball application, and PCB design/material selection are studied. The investigation focuses on four different WLP technologies: standard WLP (ball on I/O WLP), ball on polymer WLP without under bump metallurgy (UBM) layer, ball on polymer WLP with UBM layer, and encapsulated copper post WLP. Ball on I/O WLP, in which solder balls are directly attached to the metal pads on silicon wafer, is used as a benchmark for the analysis. 3-D finite element modeling is performed to investigate the effects of WLP structures, UBM layer, polymer film material properties (in ball on polymer WLP), and encapsulated epoxy material properties (in copper post WLP). Both ball on polymer and copper post WLPs have shown great reliability improvement in thermal cycling. For ball on polymer WLP structures, polymer film between silicon and solder balls creates a 'cushion' effect to reduce the stresses in solder joints. Such cushion effect can be achieved either by an extremely compliant film or a 'hard' film with a large coefficient of thermal expansion. Encapsulated copper post WLP shows the best thermo-mechanical performance among the four WLP structures. Furthermore, for a fan-out WLP, it has been found that the critical solder balls are the outermost solder balls under die-area, where the maximum thermal mismatch takes place. In a fan-out WLP package, chip size, other than package size, determines the limit of solder ball thermal cycling fatigue performance is limited by die-size. However, there has been a demand for WLP development with larger die, finer pitch and higher functionality applications.

Keywords: Wafer level packaging, solder joint thermo-mechanical reliability, finite element analysis, encapsulated copper post WLP.
of redistribution layer (RDL) process [4–7], copper post process [8], and compliant layer process [9]. These WLP structures have demonstrated the significant enhancement and improvement on solder joint reliability [4–9].

In general, there are two categories of WLP technologies: ‘fan-in’ WLP, and ‘fan-out’ WLP. In fan-in WLP packages, chip area is equal to the package area, as shown in Fig. 1. The number of I/O is limited by die-size. In order to develop ultra large array WLPs, fan-out wafer level packaging technologies have emerged recently, such as embedded wafer-level ball grid array (eWLB) technology, and redistributed chip packaging (RCP) technology [10,11]. In a fan-out WLP process, wafer reconfiguration and wafer molding technology are needed. Fan-out WLP technologies have extended WLPs to the next stage with a great extension of pin-count. Fig. 1 is a schematic for the comparison between a fan-in WLP and a fan-out WLP.

There are many factors that affect the thermo-mechanical reliability of solder joints in WLP packages. Polymer film layer, in which redistribution traces are embedded, serve as a stress buffer layer to reduce the stress level in solder joints. It is generally conceived that the high compliance of polymer film (e.g., low Young’s modulus) results in solder joint stress reduction [12]. Ball shape, geometry, standoff height, and material also play an important role in thermo-mechanical performance of WLPs [13–20]. Previous works have demonstrated that a greater standoff height with a slim ball-shape offer improved reliability performance. In addition, PCB design and material selection also contribute significantly to WLP’s reliability.

In this paper, a variety of WLP structures, which include both fan-in and fan-out WLPs, are studied for solder joint reliability performance, from a structural design point of view. Standard WLP structure, i.e., ball on I/O, is used as a benchmark to compare with other WLP configurations, such as ball on polymer WLP without UBM layer, ball on polymer WLP with UBM layer, and encapsulated copper post WLP. Finite element models for various WLP structures are developed and analyzed. The effects of WLP structures, UBM process, polymer film material properties (in ball on polymer), and encapsulated epoxy material properties (in copper post WLP), are investigated in detail. The solder joint reliability for a fan-out WLP is analyzed to compare with fan-in WLPs. Other considerations to improve solder joint reliability, such as the use of ‘dummy’ balls at corner locations, the effect of PCB design, and PCB core material selection, are also discussed in this paper.

2. Fan-in WLPs

2.1. WLP Structure A – ball on I/O structure

Ball on I/O WLP is a standard wafer level packaging technology and the process is very similar to a typical flip chip technology. As shown in Fig. 2a, the ball is attached to the aluminum pad directly through under bump metallurgy (UBM) structure. The redistribution layer (RDL) process can be added to re-route the signal path from the die peripheral I/O to the new desired bump locations, as shown in Fig. 2b. Although these two structures shown in Fig. 2 are different, the added redistribution layer and the passivation layer in Fig. 2b do not provide additional benefit to solder joint reliability performance. The solder balls in these two structures are both directly connected to silicon base. It has been well reported that WLP Structure A is limited to 6 × 6 array size (or less) at 0.5 mm pitch to meet the thermal cycling reliability requirement [3–6].
polymer dielectric film layer is placed between solder ball and silicon base. Such a layer will act as stress buffer when thermal-mechanical stress is subjected due to thermal mismatch between PCB and silicon during temperature change. Consequently, the stresses applied to solder balls will be reduced. Detailed finite element analysis will be performed in the subsequent analysis. It has been demonstrated experimentally [7] that with WLP Structure B, the array size can be extended to $12 \times 12$ with 0.5 mm pitch while meeting reliability requirement.

2.3. WLP Structure C – ball on polymer with UBM layer

Fig. 4 is a schematic of WLP Structure C for ball on polymer WLP with UBM layer. Since UBM process is added, manufacturing cost might be higher. Similar to WLP Structure B, solder balls in WLP Structure C sit on a dielectric polymer film layer to avoid a direct connection with silicon base. The effect of UBM structure will be investigated in the subsequent analysis.

2.4. WLP Structure D – encapsulated copper post WLP

Fig. 5 is a schematic of a copper post WLP structure. Thick copper pillars (~70 μm) are electroplated, followed by an epoxy encapsulation. Fig. 6 is a picture of copper post formation on wafer before molding process [8]. The difference between WLP Structure B (ball on polymer) and copper post WLP is that a thick copper/epoxy layer is placed on the top of polymer film before the ball attachment. Such a structure has demonstrated superior thermal-mechanical reliability performance.

3. Fan-out WLPs

In fan-in WLP packages, chip area is equal to the package area, thus the number of I/O is limited. In addition, fan-in WLPs are subject to front-end yield, therefore, both front-end good dies and front-end bad dies are packaged. Fan-in WLP is bare die package, which is fragile and difficult in handling during test, assembly and surface mount. Fan-out WLP eliminates those restrictions. Fig. 7 is a cross-section schematic view of fan-out WLP. Mold compound is used to carry fan-out array and protect the chip back side.

From a structural point of view, fan-out WLP is very similar to a typical ball grid array (BGA) package, in which a substrate or interposer is used. However, fan-out WLPs are substrate-less wafer level packages, which are fabricated and tested at wafer level. Fig. 8 depicts a general flow of fan-out WLP process. Wafer reconfiguration is needed with a wafer molding process.

Since a fan-out WLP is structurally similar to a BGA package, solder joint thermo-mechanical behaviors in a fan-out WLP is similar to a BGA package. The critical solder balls in a fan-out WLP are located beneath silicon chip area, where the maximum CTE mismatch occurs between silicon and PCB [21].

4. Finite element modeling

4.1. Structural model

Four fan-in WLP Structures A–D are considered first. The detailed geometry information of the four WLP structures is shown in Fig. 9. In the present study, the ball pitch for all structures is 0.5 mm, and the solder ball opening diameter on silicon side is fixed as 0.25 mm. The PCB side is assumed to be non-solder mask defined (NSMD). Other important geometrical dimensions of the four structures are shown in Table 1.
4.2. Finite element model

3-D finite element models are developed for the four WLP packages. In the present study, we consider only the equal array size of WLP packages in both directions. Thus, the one-eighth model is used, as shown in Fig. 10, according to the symmetry conditions. It is known that the outermost solder balls along the diagonal directions are the most critical ones with the largest thermo-mechanical stresses. To reduce the possible edge effect of PCB board on the outermost solder ball stresses, the PCB size in the model is extended at least 2.5 times of the package size. ANSYS 11.0 is used for finite element analysis. The SOLID45 linear element is used for meshing all the materials except solder balls. The VISCO107 linear element (8-node element), which describes the viscoplastic material behavior, is used to mesh solder balls. Detailed
finite element mesh patterns at solder ball regions for the four WLP structures are shown in Fig. 11.

Based on the experimental observations of the failure mode in solder joints under thermal cycling conditions [3], fatigue cracks occur in solder bulks at package side near the interface of solder bulk/copper or UBM layer. In order to extract the meaningful damage parameters, a fixed thickness layer of 10 μm is created in each finite element model for each WLP structure, as shown in Fig. 11.

4.3. Material model

The WLP packages are made up of different materials. A summary of the materials used in the present study is shown in Tables 2 and 3, respectively. All materials except solder alloy are modeled as linear elastic. The temperature dependency can be taken into consideration whenever the glass transition temperature $T_g$ is within the thermal cycling range of $-40 \, ^\circ C$ to $125 \, ^\circ C$. The PCB is fiber reinforced epoxies which makes the properties differ in out of

<p>| Table 2 |
| Material property details. |</p>
<table>
<thead>
<tr>
<th>Materials</th>
<th>Young's modulus (GPa)</th>
<th>Coefficient of thermal expansion (ppm/°C)</th>
<th>Poisson's ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon</td>
<td>130</td>
<td>2.6</td>
<td>0.28</td>
</tr>
<tr>
<td>Passivation</td>
<td>105</td>
<td>11</td>
<td>0.24</td>
</tr>
<tr>
<td>UBM</td>
<td>50</td>
<td>16</td>
<td>0.35</td>
</tr>
<tr>
<td>Aluminum pad</td>
<td>69</td>
<td>24</td>
<td>0.32</td>
</tr>
<tr>
<td>RDL pad</td>
<td>130</td>
<td>16.8</td>
<td>0.34</td>
</tr>
<tr>
<td>Epoxy</td>
<td>14</td>
<td>20</td>
<td>0.24</td>
</tr>
<tr>
<td>Polymer</td>
<td>1.2</td>
<td>52</td>
<td>0.34</td>
</tr>
<tr>
<td>Polymer film 1</td>
<td>1.2</td>
<td>52</td>
<td>0.34</td>
</tr>
<tr>
<td>Polymer film 2</td>
<td>1.2</td>
<td>52</td>
<td>0.34</td>
</tr>
<tr>
<td>Cu post</td>
<td>130</td>
<td>16.8</td>
<td>0.3</td>
</tr>
<tr>
<td>Solder ball</td>
<td>50</td>
<td>24.5</td>
<td>0.35</td>
</tr>
<tr>
<td>PCB pad</td>
<td>130</td>
<td>16.8</td>
<td>0.34</td>
</tr>
<tr>
<td>PCB</td>
<td>25</td>
<td>16</td>
<td>0.39</td>
</tr>
</tbody>
</table>

| Table 3 |
| Anand’s model constants for the SAC solder [23]. |
| Constant | Value |
| $s_0$, MPa | 1.3 |
| $Q/R$, K | 9000 |
| $A$, s$^{-1}$ | 500 |
| $\varepsilon$ | 7.1 |
| $m$ | 0.3 |
| $h_0$, MPa | 5900 |
| $s^*$, MPa | 39.4 |
| $n$ | 0.03 |
| $a$ | 1.5 |

Fig. 10. One-eighth finite element model for a WLP package on board.

Fig. 11. Finite element models of various WLP structures: (a) WLP Structure A; (b) WLP Structure B; (c) WLP Structure C; and (d) WLP Structure D.
plane direction. However, the isotropic properties are used here for the PCB since this study is not intended to develop a precise predictive fatigue model. The solder alloy, i.e. SAC305 alloy, is modeled as rate-dependent viscoplastic material using ANAND model [22]. Reinikainen et al. [23] has fitted constants for SAC305 alloy, and the nine constants are shown in Table 3.

4.4. Loading condition

Before subjecting the package to thermal cycling condition, stress-free temperature should be determined. There are three commonly-used initial stress-free temperature conditions. One is the solidus temperature of solder material (e.g., for SAC305, this temperature is 217°C). This condition considers that the solder joints start to provide mechanical support as soon as the solder material is solidified during the reflow process. The second option for stress-free condition is the room temperature as initial stress-free (e.g. 25°C). This assumes that the shipping and storage time is sufficiently long to relax all the residual stresses in solder joints from the assembly process. The last option for stress-free condition uses the high-dwell temperature of thermal cycle or operating conditions (denoted as $T_{\text{max}}$, e.g. = 125°C for thermal cycling from −40°C to 125°C). This assumes that after several thermal cycles, the package reaches a stabilized cyclic pattern where the lowest stresses are seen at the end of the high temperature dwell period.

Previous studies have found that, for viscous materials such as solder, regardless of initial stress-free conditions, the structure will readjust the stress state during thermal cycling and will reach a ‘near-stress-free’ at high-dwell temperature after a few cycles. The studies also showed that the stabilized values of strain or strain energy density per cycle are independent of the initial stress-free setting [24]. Since only per-cycle stabilized values are used in fatigue analysis, it was recommended to use $T_{\text{max}}$ as initial stress-free condition to achieve the stabilized solutions quickly. In the present study, 125°C is used as stress-free temperature for thermal cycling loading from −40°C to 125°C. Results showed that the stabilization is even achieved within the first cycle.

The packages are simulated with a loading profile shown in Fig. 12. The cycle time each cycle is 60 min, with 15 min during ramp up and down, and 15 min of dwell at −40°C and 125°C, respectively. Since the initial stress-free is selected as 125°C, the stabilization is achieved within the first cycle. The data reported in the subsequent analysis are based on the per-cycle data in the second cycle.

4.5. Per-cycle inelastic strain energy density

Usually, the per-cycle inelastic strain (or creep strain) or inelastic strain energy density is used as damage metrics to evaluate solder joint reliability. To prevent any mesh dependency and stress singularity effect at geometry edge, Darveaux [25] and Syed [26] have used a solid thin layer of elements near package/solder interface for volume averaging. As described previously, a 10 μm thickness layer is created for each model with two layers of elements near the interface of solder bulk/UBM layer or copper pad. The volume averaged inelastic energy density over the thin disk (Fig. 13) is defined as follows:

$$\Delta W_{\text{ave}} = \frac{\sum \Delta W_i V_i}{\sum V_i}$$

where $\Delta W_{\text{ave}}$ is the average inelastic strain energy density accumulated per cycle for fixed thickness layer elements, $\Delta W_i$ the strain energy density accumulated per cycle for each element $i$ and $V_i$ the volume of each element $i$.

It is noted that the accumulated inelastic strain density each cycle comes from the four time-periods during each cycle, i.e., ramp up and down, dwell at high temperature and low temperature respectively [27–31].

5. Modeling results

5.1. Effect of WLP structures

Fig. 14 plots the per-cycle inelastic strain energy densities for the four WLP Structures A–D, respectively, for a 12 × 12 array packages with 0.5 mm pitch. Compared to the Structure A, all other
three Structures B–D show more than 30% reduction in the accumulated inelastic strain energy density per cycle. This means that, with the incorporation of a dielectric polymer film between solder balls and silicon, and/or an encapsulated copper post layer, the stresses in solder joints can be reduced significantly compared to a ‘rigid’ connection in WLP Structure A. WLP Structure D, i.e., the encapsulated copper post WLP, shows the best performance. Experimental data have shown that Structure A WLPs can survive only up to 6 × 6 array size, while all other three structures can pass thermal cycling reliability requirement up to 12 × 12 array size [1,5]. The finite element modeling results are consistent with the experimental observations.

5.2. Effect of UBM layer

Both Structures B and C are ball on polymer WLP configurations. The difference between these two structures is that Structure B does not have UBM layer. It can be seen from Fig. 14 that the UBM layer has slightly beneficial effect on thermo-mechanical performance of solder joint reliability. Both Structures B and C show superior fatigue resistance due to the introduction of dielectric film layer between solder ball and silicon.

5.3. Effect of polymer film material properties

Polyimide film is usually used for polymers 1 and 2 in WLP Structures B and C. From Table 2, it can be seen that polyimide is very compliant with a Young’s modulus of 1.2 GPa, and a coefficient of thermal expansion of 52 × 10⁻⁶/°C respectively. The extreme compliance of polyimide film is often attributed to be the reason for thermal–mechanical performance improvement in solder joints. A parametric matrix study is performed to understand the effects of the Young’s modulus and the CTE of the film, as shown in Figs. 15 and 16, respectively. When the modulus is 1.2 GPa, which means that film is extremely compliant, the CTE of the film has negligible effect on solder joint behavior. However, when the film modulus is 100 GPa, the solder joint stress decreases significantly with the increase of the film CTE. When the CTE is above 50 × 10⁻⁶/°C, solder joint stress is even lower than that the case with the film Young’s modulus of 1.2 GPa. Such results indicate that the stress buffer effect can be realized either with an extreme compliant material or a ‘hard’ material with a relatively large CTE. For a very soft film, solder joint stresses are relieved due to the large deformation of the film. For a hard film with a larger CTE, the overall CTE of the combined silicon/film structure increases, therefore, the thermal mismatch between the silicon/film stack and the PCB is reduced, and solder joint stresses are reduced as well. The encapsulated copper post WLP structure is similar to the case of a ‘hard’ film described above. A relatively high CTE of both copper and epoxy in a copper post WLP releases thermal stresses in solder joints.

5.4. Effect of encapsulated copper post structure

The CTEs of the encapsulated epoxy and copper post in WLP Structure D are 20 × 10⁻⁶/°C and 17 × 10⁻⁶/°C, respectively, which are much greater than silicon’s CTE. Therefore, the effective CTE of the encapsulated silicon increases effectively. As a result, solder joint stresses are reduced. To understand the effect of material properties of epoxy, a parametric study is performed, as shown in Figs. 17 and 18, respectively. When the CTE of the epoxy is kept at 20 × 10⁻⁶/°C, the modulus of epoxy has a nonlinear relationship with AW. It seems an optimal value is around 70 GPa for the lowest solder joint stress. On the other hands, in Fig. 18, it can be seen that further increasing epoxy CTE from 20 × 10⁻⁶/°C to 40 × 10⁻⁶/°C will reduce stresses in solder joint, but stress will not go down further from 40 × 10⁻⁶/°C to 60 × 10⁻⁶/°C. These results show that there might be an optimal point for both CTE and modulus of the epoxy to achieve the maximum benefit of solder joint reliability improvement. By optimizing epoxy material properties, copper post WLP reliability can be further enhanced. Furthermore, it has been found that in a copper post WLP structure, the effect of the copper post/epoxy layer is more prominent than the redistribution layer on solder joint stress reduction. Without the presence of the redistribution layer in a copper post WLP structure, the per-cycle inelastic strain energy density has a slightly increase, as shown in Table 4.
5.5. Effect of fan-Out WLP structure

In Fig. 19, the per-cycle inelastic energy density is plotted against the location of solder balls in a diagonal direction for a 16\times16 array fan-out WLP package, in which 6\times6 array solder balls are under die-area. Fig. 19 shows that outermost ball right beneath silicon die has the maximum inelastic energy density among all balls. This is because the maximum local CTE mismatch is between silicon chip and the PCB. Thus the thermal stresses of solder balls beneath the chip are expected to be higher than the stresses on the outermost solder balls. The results show that fan-out WLP packages can extend the array size greatly while meeting thermo-mechanical reliability requirement.

6. Reliability enhancement by ball geometry and material optimization

Thermo-mechanical reliability of solder joints in WLP packages can also be improved by optimizing ball geometry and selecting appropriate material properties. Previous works have demonstrated that hourglass-shape solder joint has the best reliability performance during thermal cycling compared to column, barrel, and spherical-shaped joints. Another factor is the standoff height of the solder joint [18,19]. Solder joints with greater standoff height offer better reliability performance. In the following the effects of solder joint opening diameter, solder ball diameter (volume), and polymer-cored ball implementation are discussed.

6.1. Effect of solder ball opening diameter

When solder balls become the weakest link during thermal cycling, failures often take place at solder bulk near solder ball/package interface. It becomes obvious that increasing the contact area, the solder ball opening diameter, is the most direct way to improve the solder joint reliability. In Table 5, the per-cycle inelastic strain energy density is shown for various solder ball opening diameters. A larger diameter increases the total contact/interface area, and therefore it takes a longer time for solder ball crack propagations throughout contact interface. It is noted that such a conclusion is reached with a fixed ball diameter assumption. It will be shown next that increasing solder ball diameter will reduce the thermo-mechanical reliability.

6.2. Effect of solder ball volume (solder ball diameter)

When the solder ball opening size is fixed, the optimization of solder ball shape and volume has a great impact on solder joint reliability. Fig. 20 shows three scenarios of solder ball shapes. The larger solder ball diameter means more solder volume, which intuitively may provide stronger support for solder ball against fatigue failures. Finite element analysis has been performed on those three scenarios and the results of per-cycle inelastic strain energy density are tabulated in Table 6. It shows that the convex shape solder ball (more solder volume with a larger diameter) will result in the worst solder joint reliability performance.

It seems that contradicting results are obtained for solder ball opening diameter versus solder ball volume. When solder volume is reduced, WLP structures become more flexible to move during thermal cycling. This will result in less stresses developed at the neck area (package/silicon interface). Although less solder volume induces a greater stress in the middle portion of solder balls, the stress level at the outermost solder balls becomes lower, which results in lower thermo-mechanical stresses.

Table 4

<table>
<thead>
<tr>
<th>RDL Layer</th>
<th>Effect of RDL Layer in a Copper Post WLP Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>No RDL</td>
<td>1.0</td>
</tr>
<tr>
<td>With RDL</td>
<td>0.96</td>
</tr>
</tbody>
</table>

Table 5

<table>
<thead>
<tr>
<th>Solder Ball Opening Diameter ((\mu m))</th>
<th>(\Delta W/\Delta W_0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>200</td>
<td>1.93</td>
</tr>
<tr>
<td>250</td>
<td>1.0</td>
</tr>
<tr>
<td>300</td>
<td>0.57</td>
</tr>
</tbody>
</table>
neck area is reduced. Therefore, hourglass-shape solder joint shows the best reliability performance. On the other hands, When solder volume is fixed, local enhancement at the neck area can improve reliability performance greatly, such as the increase of solder ball opening diameter.

6.3. Effect of plastic cored solder balls

A plastic core solder ball consists of a large polymer core coated by a copper layer and covered with eutectic and/or lead-free solder. The main advantages of such a system are higher reliability due to the relaxing of stress by the polymer core and a defined ball height after reflow [13–15]. These balls could improve the solder ball reliability significantly due to the compliant feature of balls. Fig. 21 is a schematic of horizontal view of polymer core ball. Fig. 22 shows the photos of the plastic core solder balls. Table 7 shows the comparison of Young’s modulus of polymer core material and SnPb. It can be seen that polymer core material has only 1/10th of the modulus of SnPb, which will make the structure more flexible when subjected to temperature cycling.

Fig. 23 is the Weibull plot of temperature cycling results for the comparison of polymer-cored ball and conventional solder balls [14]. It clearly indicates that the plastic core solder ball structures improve the fatigue life significantly. The Young’s modulus of plastic core is much smaller than that of metal, so it is superior in relaxing the thermal stress and enables much greater resistance to micro-cracks in the solder layer than that of conventional solder balls.

7. Other considerations for solder ball reliability enhancement in WLPs

7.1. Implementation of dummy solder balls

It has been well understood that the outermost corner solder balls in diagonal directions are subjected to the maximum inelastic deformation during thermal cycling, and therefore, fail first. For large array WLP packages, making corner balls non-electrically connected can improve package thermo-mechanical reliability. Two daisy chain loops were designed, as shown in Fig. 24 [3]. Corner daisy chain loops include only eight corner balls, while center daisy chain loop connects all other balls. A comparison of failure data under thermal cycling for corner and non-corner balls are shown in Table 8 [3]. It is observed that the non-corner balls have 40% longer fatigue life than corner daisy chain loop. In other words, making the corner balls non-electrically connected will improve the fatigue life dramatically by 40%. Fig. 25 plots the per-cycle normalized inelastic strain energy density map for all solder balls in a 12 x 12 array WLP package. The inelastic strain energy density

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Table 6
Effect of solder ball volume (diameter).

<table>
<thead>
<tr>
<th>Legs</th>
<th>Solder ball diameter (µm)</th>
<th>ΔW/ΔW₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>Leg 1</td>
<td>260</td>
<td>0.77</td>
</tr>
<tr>
<td>Leg 2</td>
<td>310</td>
<td>1</td>
</tr>
<tr>
<td>Leg 3</td>
<td>360</td>
<td>1.19</td>
</tr>
</tbody>
</table>

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Fig. 20. Three scenarios of solder ball shapes with the fixed solder ball opening size and ball height.

Fig. 21. Cross-section structure of polymer core ball.

Fig. 22. Real images of plastic core solder balls on WLP [14].
decays rapidly both along die edge and diagonal direction towards package center. This agrees very well with the test results.

7.2. Effect of PCB

Thermal–mechanical stresses developed in solder joints are induced by the thermal mismatch between PCB and silicon. Lowering the CTE of PCB can also reduce the stresses in solder joints. Fig. 26 shows the results of inelastic strain energy density for three sets of PCB CTEs. When low CTE PCB core material is used, the fatigue life can be increased greatly.

It has been demonstrated that a polymer film layer between solder balls and silicon with a larger CTE can increase the overall effective CTE of silicon assembly, and thus reduce the thermal stresses in solder joints. Similar concept can be developed at PCB side to include a layer of material between PCB and solder balls. The detailed studies will be reported separately.

8. Concluding remarks

Four types of fan-in WLP structures are studied first to investigate the effect of WLP structures on solder joint reliability. These four WLP structures are: standard WLP (bump on I/O), bump on polymer WLP without UBM layer, bump on polymer WLP with UBM layer, and encapsulated copper post WLP. Finite element modeling results for these WLP structures show that ball on polymer WLP, and copper post WLP have a greater improvement

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### Table 7
Material properties for polymer core material and SnPb solder.

<table>
<thead>
<tr>
<th>Material</th>
<th>Young’s modulus (GPa)</th>
<th>Poisson’s ratio</th>
<th>CTE (ppm/°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Plastic core material</td>
<td>4.7</td>
<td>0.38</td>
<td>40.2/46.2</td>
</tr>
<tr>
<td>Solder (SnPb)</td>
<td>40.2</td>
<td>0.4</td>
<td>24.7</td>
</tr>
<tr>
<td>Substrate Board</td>
<td>24.5</td>
<td>0.3</td>
<td>14</td>
</tr>
</tbody>
</table>

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### Table 8
Normalized characteristic fatigue life for failures of corner and non-corner balls [3].

<table>
<thead>
<tr>
<th>Solder ball groups</th>
<th>Corner group</th>
<th>Non-corner group</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normalized characteristic life</td>
<td>1</td>
<td>1.4</td>
</tr>
</tbody>
</table>

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Fig. 23. Weibull plot of the performance of polymer core balls compared to the conventional solder balls [14].

Fig. 24. Two daisy chain loops design.

Fig. 25. Normalized inelastic strain energy density per cycle for a one eighth part of a 12 × 12 array WLP package.

Fig. 26. Effect of PCB CTE on solder joint reliability.
in thermo-mechanical reliability performance over the bump on I/O WLPs. In a ball on polymer WLP structure, polymer film between silicon and solder balls creates a ‘cushion’ effect to reduce the stresses in solder joints. Such cushion effect can be achieved either by an extremely compliant film or a ‘hard’ film with large coefficient of thermal expansion. In the later case, the reduction of solder joint stresses is due to the overall increase of the combined film/wafer effective CTE. It has been found that a ‘hard’ layer with a large CTE can reduce solder joint stress beyond a compliant film. This has been validated by an encapsulated copper post WLP structure, which shows the best performance on all four structures in terms of solder joint reliability, experimentally and numerically.

Fan-out WLPs are structurally similar to BGA packages. Therefore, the critical solder balls are not on the outermost corners along package diagonal directions. The outermost solder balls under die-area are most critical since the maximum thermal mismatch takes place at die-shadow location. For fan-out WLP packages, chip size, other than package size, determines the limit of solder joint reliability.

Ball geometry and materials play important roles in enhancing solder joint reliability. The more compliant solder ball is, the greater thermo-mechanical reliability is achieved. Therefore, reducing individual solder ball volume or using more compliant materials such as polymer-cored solder balls will improve reliability performance. On the other hands, since failures are often at solder bulk near package/solder interface region, local enhancement methods, such as the increase of solder ball opening diameter, will be beneficial in reliability performance.

Solder balls often start to crack at the corner locations along package diagonal directions. Both experimental and finite element analysis have demonstrated that making corner balls non-electrically connected can improve the WLP thermo-mechanical reliability significantly.

References